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# 350W, 50V High Power RF LDMOS FETs

# **Description**

The MK1320V is a 350-watt, internally matched LDMOS FETs, designed for applications including cooking, heating and medical with frequencies from 1000 to 1400 MHz.

It can be used for 1300MHz particle accelerator CW application, avionics and L band commercial pulse application.

•Typical Performance (on Innogration fixture with device soldered): Tcase = 25 degree C, Pulse CW signal, 100us 20% duty cycle, DD=50V, Idq=100mA

Freq(MHz)	P1(dBm)	P3(dBm)	P3(W)	EFF(%)@P3	Gain (dB)@P1
1300	55	55 56		57.5	19

### CW signal, VDD=50V, Idq=100mA

Freq(MHz)	Pout(W)	Eff(%)	Power Gain(dB)
1300	340	53	16.7

### **Features**

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- . Input internally matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- · Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

## **Table 1. Maximum Ratings**

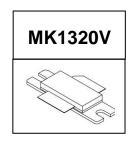
Rating	Symbol	Value	Unit
DrainSource Voltage	$V_{\scriptscriptstyle DSS}$	125	Vdc
GateSource Voltage	$V_{\sf GS}$	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T,	+225	°C

# **Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case (See note 1)			
Tcase= 85°C, 1300MHz,100us, 20% duty cycle, 50V,	ZeJC	0.05	°C/W
Idq=100mA			

#### **Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2



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Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage	V		125		V
(V <sub>GS</sub> =0V; I <sub>D</sub> =100uA)	V <sub>DSS</sub>		125		V
Zero Gate Voltage Drain Leakage Current				10	^
$(V_{DS} = 50V, V_{GS} = 0 V)$	I <sub>DSS</sub>			10	μА
GateSource Leakage Current	_			1	^
$(V_{GS} = 6 \text{ V}, V_{DS} = 0 \text{ V})$	I <sub>GSS</sub>			ı	μΑ
Gate Threshold Voltage	$V_{GS}(th)$		1.6		V
$(V_{DS} = 50V, I_D = 600 \text{ uA})$	V <sub>GS</sub> (III)		1.0		V
Gate Quiescent Voltage	V		2.1		V
$(V_{DD} = 50V, I_{DQ} = 100 \text{ mA}, \text{ Measured in Functional Test})$	$V_{GS(Q)}$		2.1		V

Functional Tests (In Innogration Test Fixture, 50 ohm system) : $V_{DD}$  =50 Vdc,  $I_{DQ}$  = 100mA, f = 1300 MHz, Pulsed CW Signal Measurements(100us, 10%). Pin=4W

Output Power	P <sub>out</sub>	320	W
Power Gain	Gp	19	dB
Drain Efficiency@Pout	η <sub>ο</sub>	55	%
Input Return Loss	IRL	-7	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system):  $V_{DD} = 50 Vdc$ ,  $I_{DQ} = 100 mA$ , f = 1300 MHz

VSWR 10:1 at 320W pulse CW Output Power	No Device Degradation
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Figure 1: RF Pulsed CW sweep (Vdd=50V, Idq=100maA, 100us, 10%)

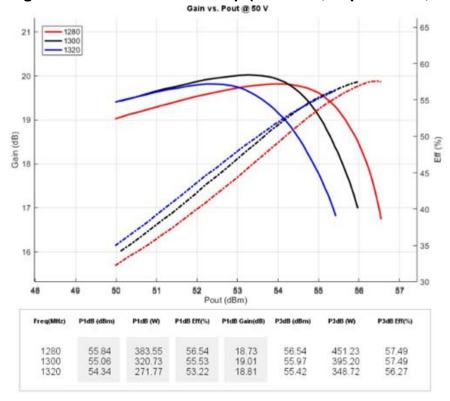
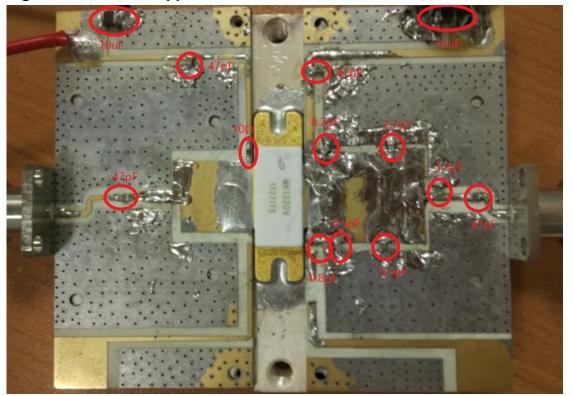


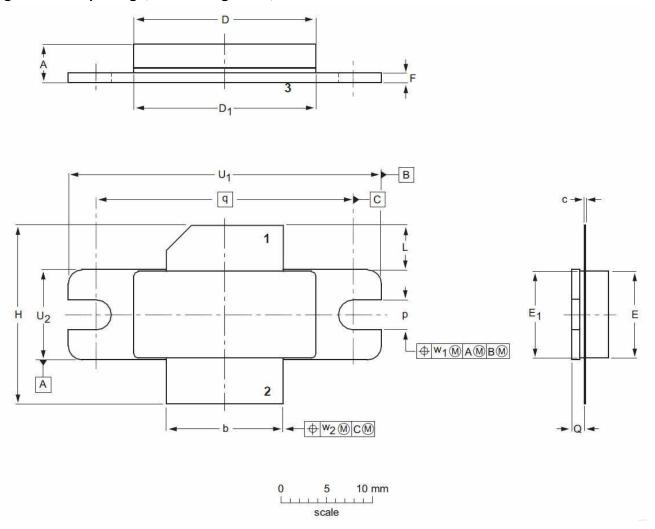
Figure 2: Picture of application fixture





# **Package Outline**

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	Α	b	С	D	D <sub>1</sub>	E	E <sub>1</sub>	F	н	L	р	Q	q	Uı	U <sub>2</sub>	W <sub>1</sub>	$W_2$
	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	07.04	34.16	9.91	0.05	0.54
mm	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45	27.94 33.91	9.65	5 0.25	0.51	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	4.400	1.345	0.390	0.04	0.00
inches	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057	1.100	0.380	0.01	0.02	

OUTLINE		REFERENCE	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	IOOOL DATE
PKG-B2E					03/12/2013



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# **Revision history**

**Table 5. Document revision history** 

Date	Revision	Datasheet Status
2017/3/31	V1	Preliminary Datasheet Creation
2017/7/14	V2	Modified test data

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